NETTHREADS-10G: SOFTWARE PACKET PROCESSING ON NETFPGA-10G IN A VIRTUALIZED NETWORKING ENVIRONMENT

DEMONSTRATION ABSTRACT

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FPGAs are often used in high speed networking and telecommunications environments, where they have been shown to be very capable of line rate forwarding and routing. However, complex processes are more easily described in high-level software. In addition, many researchers do not have backgrounds in complex hardware design. NetThreads10G is a solution to both of these problems – a soft, multithreaded multicore network processor implemented on the NetFPGA-10G[1], and software programmable using C. NetThreads10G is a port and upgrade of the original NetThreads [2] system designed for the NetFPGA: the number of cores has been doubled, packet buffer capacity increased, and a new Ethernet packet based programming system has been implemented.

NetThreads10G has a bus-based architecture connecting four MIPS-like processors to a shared data cache and a shared packet I/O buffer (Figure 1). Each core has a private instruction cache and four independent threads executed in a round robin fashion. Sixteen hardware locks are included for protecting critical code sections. The NetFPGA-10G onboard RLDRAM provides up to 128MB of main memory.

During the demonstration, a sample application is developed and compiled using the NetThreads cross compiler tool. NetThreads10G is configured on the NetFPGA10G, and the application is downloaded remotely via Ethernet packets. The application is a *deep packet inspection* program that can detect suspicious keywords in packet payloads and keeps a record in shared memory. The demo shows how NetThreads affords us complete programmable and stateful control over OSI Layer 2 and above.

The demonstration also shows NetThreads in the context of the SAVI (Smart Applications on Virtual Infrastructure) testbed. SAVI [3] is a new approach to network and Internet infrastructure - completely virtualized and extremely flexible, it views infrastructure as "converged", where processing, compute, networking and reconfigurable resources are all part of a shared and managed pool. Having reconfigurable hardware in such a virtualized and programmable environment will open up new avenues of research in reconfigurable systems.

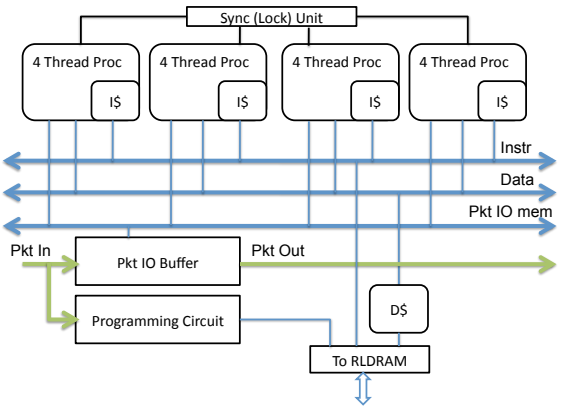

Fig. 1. The architecture of NetThreads10G

References

[1] "Netfpga-10g," http://netfpga.org/10G_specs.html, accessed: 2013-07-03.

[2] M. Labrecque, J. G. Steffan, G. Salmon, M. Ghobadi, and Y. Ganjali, "NetThreads: Programming NetFPGA with Threaded Software," in *NetFPGA Developers Workshop*, vol. 9, 2009.

[3] M. Smit, J. Ng, M. Litoiu, G. Iszali, and A. Leon-Garcia, "Smart Applications on Virtual Infrastructure," in *Proceedings of the 2011 Conference of the Center for Advanced Studies on Collaborative Research*, ser. CASCON '11. Riverton, NJ, USA: IBM Corp., 2011, pp. 381–381.

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